KHENTAWAS, FARRUKHNAGAR, GURGAON, HR

Department: EEE

Academic Session: (MAY- AUG 2021)

Lesson Plan with Assignment questions

Subject with code:CMOS Design(PCC-ECE308G)

Name of Faculty with designation : Dr. Ekta Thakur, Assistant Professor

Month	Date & Day	Sem-Class	Unit	Topic/Chapter covered	Write Lecture Wise Questions	Remarks
May		VI ECE	I	Introduction of MOS Transistor,MOS Transistor, CMOS logic, .	Q1) Question related to mos Q2) Question related to CMOS	
May		VI ECE	I	Layout Design Rules, Gate Layouts,	Q1) Question related to NOR,OR Truth tables Q2) Question related to design	
May		VI ECE	I	Stick Diagrams, Long-Channel I-V characteristics,	Q1) Question related toIV Charateristics Q2) Question related to diagram	
June		VI ECE	I	C-V characteristics, Non ideal I-V Effects,	Q1) Question related to I-V Effect Q2) Question related toC-V characteristic	
June		VI ECE	I	Elmore Delay	Q1) Question related to delay Q2) Question related to delay	
June		VI ECE	I	Linear Delay Model	Q1) Question related to linear Q2) Question related to delay	
June		VI ECE	I	Logical effort	Q1) Question related logical effort Q2) Question related to array	
June		VI ECE	I	Parasitic Delay	Q1) Complexity analysis of parastic delay Q2) Complexity analysis of delay	
June		VI ECE	I	Delay in Logic Gate,Scaling.	Q1) Complexity analysis of scaling Q2) Complexity analysis ofgates	
June		VI ECE	II	Combinational Circuit Design,Circuit Families:	Q1) Complexity analysis of various circuits Q2) Applications of design	
June		VI ECE	II	Static CMOS,	Q1) Complexity analysis of cmos Q2) Applications of Static	
June		VI ECE	I	Ratioed Circuits	Q1) Complexity analysis of cmos Q2) Applications of Static	
July		VI ECE	I	Cascode Voltage Switch Logic	Q1) Numerical Q2) Numerical	
July		VI ECE	I	Dynamic Circuits, Pass Transistor Logic	Q1) Numerical Q2) Numerical	
July		VI ECE	II	Transmission Gates	Q1) Complexity analysis of gate Q2) Complexity analysis ofgates	

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July		VI ECE	II	Domino, Dual Rail Domino	Q1) Numerical Q2) Numerical	
July		VI ECE	II	CPL, DCVSPG,DPL, Circuit Pitfalls	Q1) Numerical Q2) Numerical	
July		VI ECE	II	Power: Dynamic Power, Static Power	Q1) Numerical Q2) Numerical	
July		VI ECE	II	Low Power Architecture	Q1) Numerical based on deletion operation Q2) Comparison of various operations using linked list and	
July		VI ECE	II	Interconnect: Interconnect Modelling and Impact	Q1) Question related architecture Q2) Question related to power	
July		VI ECE	III	Sequential Circuit Design Static latches and Registers Dynamic latches	Q1) Question related seqentail circuits Q2) Question related to latches	
July		VI ECE	III	Registers, Pulse Registers	Q1) Numerical Q2) Numerical	
August		VI ECE	III	Pipelining,	Q1) Numerical Q2) Numerical	
August		VI ECE	III	Schmitt Trigger,Monostable Sequential Circuits,	Q1) Numerical Q2) Numerical	
August		VI ECE	III	Astable Sequential Circuits	Q1) Question related astable Q2) Question related to circuits	
August		VI ECE	III	Timing Issues: Timing Classification of Digital System,	Q1) Numerical Q2) Numerical	
August		VI ECE	III	Modeling of Coupled Electromechanical Systems:	Q1) Numerical Q2) Numerical	
August		VI ECE	IV	Implementation of of simple microcomputer system	Q1) Numerical Q2) Numerical	
August		VI ECE	IV	Data Paths, Adders, Multipliers, Shifters, ALUs, power and speed tradeoffs	Q1) Question related multipliers Q2) Question related to shifters	
August		VI ECE	IV	Case Study: Design as a tradeoff,Memory Architectures and Building Blocks, Memory Core, Memory Peripheral Circuitry	Q1) Complexity analysis of tradeoff,architectures	